

Abstract of the Disclosure

A method of manufacturing a capacitor includes sequentially forming a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer over a semiconductor substrate. A first post-annealing of the substrate is performed under an inert atmosphere at a first temperature, and then a second post-annealing is performed at a second temperature. The first and second post annealings can be performed after forming the high dielectric layer, the plate electrode, or the interdielectric layer, or any combination thereof, as long as the second post-annealing is performed after the first post-annealing. The post-annealings are not necessarily performed in a same place or stage. The first temperature may be about 600°C to 900°C, and the second temperature about 100°C to 600°C. As a result, the dielectric constant of the high dielectric layer is increased, and leakage current is reduced.

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A method is provided for manufacturing a capacitor of a semiconductor device in which a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer are sequentially formed over a semiconductor substrate. This method includes the steps of performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature and then performing a second post-annealing of the semiconductor substrate at a second temperature. The first and second post annealing steps can be performed after the deposition of the high dielectric layer, the plate electrode, or the interdielectric layer, or any combination of this, so long as the second post-annealing step is performed after the first post-annealing step. The two post-annealing steps do not have to be performed in the same place or at the same stage during the fabrication process. The first temperature is preferably in the range of about 600°C to 900°C, and the second temperature is preferably in the range of about 100°C to 600°C. In this way, the dielectric constant of the high dielectric layer is increased, and the leakage current is reduced.